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WHAT IS CLAIMED IS:

Sub

A.

1. A data processing apparatus for executing multiple instruction sets comprising:
 - a memory, for storing a plurality of instruction words of the instruction sets;
 - 5 a processor core, for executing a primary instruction word of the instruction words;
 - a program counter register (PC), for addressing a next instruction word stored in the memory;
 - a plurality of data registers, for storing data of the instruction words;
 - 10 a processor status register, for storing the status of the processor core, wherein the processor status register contains an instruction set selector (ISS) for indicating a current instruction set of the instruction sets;
 - a predecoder, for translating at least one of the instruction sets to the primary instruction word and outputting therewith;
 - 15 an Icache, for storing the primary instruction word;
 - a decoder, for decoding the primary instruction word, wherein the processor core is used for executing the primary instruction word decoded by the decoder;
 - a program counter control, responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word different from
 - 20 the primary instruction word; and
 - a bus, being an interface between the predecoder and the memory.
2. The apparatus of claim 1, wherein there are two parts of bits in each of the data registers, at least one bit is viewed as an instruction set selection bit (IS) and the other bits stored in the data register is viewed as a target address (TA).

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3. The apparatus of claim 2, wherein the target address is a starting address of the instruction set.

4. The apparatus of claim 2, wherein the ISS is set by a specified branch instruction according to the IS in the data registers.

5. The apparatus of claim 1, wherein the predecoder contains at least one sub-decoder, for translating at least one of the instruction sets to the primary instruction word.

6. The apparatus of claim 1, wherein the sub-decoder switching is controlled by the ISS and the output of the predecoder is the primary instruction word.

10 7. The apparatus of claim 1, wherein the bit width of the primary instruction word is not equal to other instruction words, the Icache adds a recognized bit and translates the PC value to point out a relative primary instruction word.

8. The apparatus of claim 1, wherein the instruction set selector includes at least one bit.

15 9. The apparatus of claim 8, wherein the instruction set selector can be set by a specified branch instruction according to one or more instruction set bits of the data registers.